

Amendments to the Claims

1 (Presently Amended) A combiner processor comprising:
a sliding correlator for correlating a serial stream of
5 baseband symbols against a first codeword and forming a
correlation peak output;
a training decision function coupled to said
correlation peak output and generating a window output that
is asserted at the start of an interval and unasserted at
10 the end of said interval and also a training decision
output;
a demultiplexer coupled to said correlation peak output
and having a learn control input whereby when said
demultiplexer learn control input is asserted:
15 said correlation peak output is coupled to a channel
profile memory such that said correlation peak output is
added to the contents of said channel profile memory when
said training decision output is true and said correlation
peak output is inverted and added to the contents of said
channel profile memory when said training decision output is
20 false;
and when said demultiplexer learn control input is not
asserted:
said correlation peak output is multiplied with the
25 complex conjugate of the contents of said channel profile

Amendment filed under 37 CFR 1.111

memory and coupled to an accumulator which adds said multiplier result ~~during when each~~said window output is asserted and generates a decision output ~~at the end of each~~when said window output is unasserted.

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2 (Currently amended) The combiner processor of claim 1
wherein said first codeword is 11 bits.

10 3 (Currently amended) The combiner processor of claim 1
where said first codeword is a Barker codeword.

4 (Currently amended) The combiner processor of claim 1
wherein said first codeword is $\{+1, -1, +1, +1, -1, +1, +1, +1, -1, -1\}$.

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5 (Currently amended) The combiner processor of claim 1
wherein said first codeword is $\{-1, +1, -1, -1, +1, -1, -1, +1, +1, +1\}$.

20 6 (Currently amended) The combiner processor of claim 1
wherein said serial stream of baseband symbols includes Barker codewords.

7 (Currently amended) The combiner processor of claim 1
wherein said serial stream of baseband symbols includes an
in-phase component and a~~s~~is quadrature component.

5 8 (Currently amended) The combiner processor of claim 7
wherein said serial stream of quadrature symbols includes an
I channel and a Q channel.

10 9 (Currently amended) The combiner processor of claim 1
wherein said training decision function window output ~~has~~ is
asserted for a duration substantially equal to the duration
of said codeword.

15 10 (Currently amended) The combiner processor of claim 1
wherein said training decision function window output
includes is asserted when pre-cursor symbols are arriving
prior to the largest said correlation peak in said window
output asserted duration.

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11 (Currently amended) The combiner processor of claim 1
wherein said training decision function window includes
post-cursor symbols arriving after the largest said
correlation peak in said window output asserted duration.

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Amendment filed under 37 CFR 1.111

Last saved 7/10/2007 11:59:00 AM

12 (Currently amended) The combiner processor of claim 1
wherein said training decision output indicates which said codeword was received during said window output asserted duration.

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13 (Currently amended) The combiner processor of claim 1
wherein said demultiplexer learn input is asserted during a first interval.

10 14 (Currently amended) The combiner processor of claim 13 wherein said first interval occurs during the preamble of a received packet.

15 15 (Currently amended) The combiner processor of claim 13 wherein said first interval is greater than 10 said codeword symbols.

20 16 (Currently amended) The combiner processor of claim 1
wherein said baseband symbols have an in-phase component and a quadrature component and said complex conjugate comprises negating the value of said quadrature component. ~~the Q channel.~~

17 (Currently amended) The combiner processor of claim 1
wherein said channel profile memory is synchronized to said
training decision function window output.

5 18 (Currently amended) The combiner processor of claim 1
wherein said channel profile memory comprises a random
access memory and a memory controller coupled to said random
access memory.

10 19 (Currently amended) The combiner processor of claim 1
wherein said correlation peak output has an in-phase
component and a quadrature component, and said channel
profile memory has associated in-phase storage and
quadrature storage such that said correlation peak output
15 in-phase component is added to said in-phase storage and
said correlation peak output adds quadrature component is
added in said quadrature storage said when said
demultiplexer learn input is asserted.

20 20 (Currently amended) The combiner processor of claim 1
wherein said channel profile memory is initialized when said
demultiplexer learn control input is first asserted.

21 (Currently amended) The combiner processor of claim 1
wherein said channel profile memory has a number of
locations equal to the number of samples in said codeword.

5 22 (Currently amended) The combiner processor of claim 1
wherein said accumulator includes a memory which is
initialized at the start of each said window.

10 23 (Currently amended) The combiner processor of claim 1
wherein said accumulator includes a memory and an adder
which adds the current said multiplier output to said memory
contents.

15 24 (Currently amended) The combiner processor of claim 1
wherein said decision output compares said accumulated value
against a threshold at the end of said window.

20 25 (Currently amended) The combiner processor of claim
24 wherein said threshold is 0.

26 (Currently amended) A combiner processor having two
states:

a training state whereby a serial stream of baseband
symbols is correlated against a first codeword, thereby
25 producing a correlation peak output, said correlation peaks
Amendment filed under 37 CFR 1.111

examined by a training decision function to generate a window output indicating the extent of said symbol and a decision output which is either true or false, said correlation peaks added to a channel profile memory when 5 said decision output is true and inverted and added to said channel profile memory when said decision output is false;

a decision state whereby ~~said serial stream of baseband symbols~~ correlation peak output is multiplied by the complex conjugate of the contents of said channel profile memory to 10 produce a multiplier output;

an accumulator coupled to said multiplier output whereby wherein ~~said adder~~ accumulator is reset at the start of said window, accumulates the output of said multiplier during said window, and generates a binary output value at 15 the end of said window.

27 (Currently amended) The combiner processor of claim 26 wherein said first codeword is 11 bits.

20 28 (Currently amended) The combiner processor of claim 26 wherein said first codeword is a Barker codeword.

29 (Currently amended) The combiner processor of claim 26 wherein said first codeword is {+1, -1, +1, +1, -1, +1, +1, +1, -1, -1, -1}.

Amendment filed under 37 CFR 1.111

30 (Currently amended) The combiner processor of claim
26 wherein said first codeword is {-1,+1,-1,-1,+1,-1,-1,-
1,+1,+1,+1}.

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31 (Currently amended) The combiner processor of claim
26 wherein said serial stream of baseband symbols includes
Barker codewords.

10 32 (Currently amended) The combiner processor of claim
26 wherein said serial stream of baseband symbols is two
streams of symbols in quadrature phase.

33 (Currently amended) The combiner processor of claim
15 32 wherein said serial stream of quadrature phase symbols
includes an I channel and a Q channel.

34 (Currently amended) The combiner processor of claim
20 26 wherein said training decision function window output has
a duration equal to the duration of said codeword.

35 (Currently amended) The combiner processor of claim
26 wherein said training decision function window output

includes pre-cursor symbols arriving prior to the largest said correlation peak in said window.

36 (Currently amended) The combiner processor of claim
5 26 wherein said training window includes post-cursor symbols arriving after the largest said correlation peak in said window.

37 (Currently amended) The combiner processor of claim
10 26 wherein said training decision output indicates which said codeword was received during said window.

38 (Currently amended) The combiner processor of claim
26 wherein said training state occurs during a first
15 interval.

39 (Currently amended) The combiner processor of claim
38 wherein said first interval occurs during the preamble of a received packet.

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40 (Currently amended) The combiner processor of claim
38 wherein said first interval is greater than 10 said codeword symbols.

41 (Currently amended) The combiner processor of claim
26 33 wherein said complex conjugate comprises negating the
value of thesaid Q channel.

5 42 (Currently amended) The combiner processor of claim
26 wherein said channel profile memory is synchronized to
said training decision function window output.

10 43 (Currently amended) The combiner processor of claim
26 wherein said channel profile memory comprises a random
access memory and a memory controller coupled to said random
access memory.

15 44 (Currently amended) The combiner processor of claim
26 wherein said channel profile memory adds quadrature said
correlation peak output when said demultiplexer learn input
is asserted.

20 45 (Currently amended) The combiner processor of claim
26 wherein said channel profile memory is initialized at the
beginning of said training state.

25 46 (Currently amended) The combiner processor of claim
26 wherein said channel profile memory has a number of
locations equal to the number of samples in said codeword.
Amendment filed under 37 CFR 1.111

47 (Currently amended) The combiner processor of claim
26 wherein said accumulator includes a memory which is
initialized at the start of each said window.

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48 (Currently amended) The combiner processor of claim
26 wherein said accumulator includes a memory and an adder
which adds the current said multiplier output to said memory
contents.

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49 (Currently amended) The combiner processor of claim
26 wherein said binary output compares said accumulated
value against a threshold at the end of said window.

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50 (Currently amended) The combiner processor of claim
49 wherein said threshold is 0.

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51 (Currently amended) The combiner processor of claim
26 wherein said decision state occurs during a second
interval.

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52 (Currently amended) A process for generating a
decision output from a serial stream of baseband symbols,
said process comprising:

a first learning step comprising:

Amendment filed under 37 CFR 1.111

correlating said incoming serial stream with one or
more codewords to generate a correlation output, examining
~~the~~ said correlation output to generate a training decision
which is positive or negative, and also generating a window
5 signal indicating the start and end of said incoming serial
symbols, said incoming symbols added to the contents of a
channel profile memory when said training decision is
positive, and inverting said incoming symbols and adding to
the contents of said channel profile memory when said
10 training decision is negative;

a second decision step comprising:

multiplying said correlation peaks with the complex
conjugate of said channel profile memory contents, thereby
forming a multiplier output and accumulating said multiplier
15 output during said window signal start time to said window
signal end time to form a decision value, and comparing said
decision value at the said window signal end time to form
said decision output.

20 53 (Currently amended) The process of claim 52 wherein
said first codeword is 11 bits.

54 (Currently amended) The process of claim 52 wherein
said first codeword is a Barker codeword.

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Amendment filed under 37 CFR 1.111

Last saved 7/10/2007 11:59:00 AM

55 (Currently amended) The process of claim 52 wherein
said first codeword is $\{+1, -1, +1, +1, -1, +1, +1, +1, -1, -1, -1\}$.

56 (Currently amended) The process of claim 52 wherein
5 said first codeword is $\{-1, +1, -1, -1, +1, -1, -1, +1, +1, +1\}$.

57 (Currently amended) The process of claim 52 wherein
said serial stream of baseband symbols includes Barker
codewords.

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58 (Currently amended) The process of claim 52 wherein
said serial stream of baseband symbols ~~is~~ has quadrature
phase separation.

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59 (Currently amended) The combiner processor of claim 7
wherein said serial stream of quadrature phase symbols
includes an I channel and a Q channel.

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60 (Currently amended) The process of claim 52 wherein
said window output has duration equal to the duration of
said codeword.

61 (Currently amended) The process of claim 52 wherein
said window output includes pre-cursor symbols arriving
prior to the largest said correlation peak in said window.

5 62 (Currently amended) The process of claim 52 wherein
said window includes post-cursor symbols arriving after the
largest said correlation peak in said window.

10 63 (Currently amended) The process of claim 52 wherein
said training decision output indicates which said codeword
was received during said window.

15 64 (Currently amended) The process of claim 52 wherein
said learning step precedes said decision step.

65 (Currently amended) The process of claim 52 wherein
said learning step occurs during the preamble of a received
packet.

20 66 (Currently amended) The process of claim 52 wherein
said learning step uses more than 10 said codeword symbols.

25 67 (Currently amended) The process of claim 52 59
wherein said complex conjugate comprises negating the value
of the said Q channel.

Amendment filed under 37 CFR 1.111

68 (Currently amended) The process of claim 52 wherein
said channel profile memory is synchronized to said window.

5 69 (Currently amended) The process of claim 52 wherein
said channel profile memory comprises a random access memory
and a memory controller coupled to said random access
memory.

10 70 (Currently amended) The process of claim 52 wherein
said correlation output has an in-phase component and a
quadrature component, and said channel profile memory has
in-phase storage and quadrature storage such that said
correlation output in-phase component is added to said in-
15 phase storage and said correlation output quadrature
component is added to said quadrature storage—adds
~~quadrature said correlation peak output during said learning~~
step.

20 71 (Currently amended) The process of claim 52 wherein
said channel profile memory is initialized at the beginning
of said learning step.

72 (Currently amended) The process of claim 52 wherein
said channel profile memory has a number of locations equal
to the number of samples in said codeword.

5 73 (Currently amended) The process of claim 52 wherein
said accumulation includes a memory which is initialized at
the start of each said window.

10 74 (Currently amended) The process of claim 52 wherein
said accumulation includes a memory and an adder which adds
the current said multiplier output to said memory contents.

15 75 (Currently amended) The process of claim 52 wherein
said decision value compares said accumulated value against
a threshold at the end of said window.

20 76 (Currently amended) The combiner processor of claim
24 wherein said threshold is 0.

20 77 (Currently amended) A combiner processor comprising:
 a sliding correlator for correlating a serial stream of
 baseband symbols against a first codeword and forming a
 correlation peak output;

a training decision function coupled to said correlation peak output and generating a window output that is asserted during an interval, and unasserted at other times, the training decision function also generating and a
5 training decision output;

said correlation peak output is coupled to a channel profile memory such that said correlation peak output is added to said channel profile memory when said training decision output is true and said correlation peak output is
10 inverted and added to said channel profile memory when said training decision output is false; and

a decision control input whereby when said decision control input is asserted, said correlation peak output is multiplied with the complex conjugate of said channel profile memory and coupled to an accumulator which adds said multiplier result during each when said window output is asserted and generates a decision output at the end of each when said window output is unasserted.

20 78 (Currently amended) The combiner processor of claim
77 wherein said first codeword is 11 bits.

79 (Currently amended) The combiner processor of claim
77 wherein said first codeword is a Barker codeword.

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Amendment filed under 37 CFR 1.111

Last saved 7/10/2007 11:59:00 AM

80 (Currently amended) The combiner processor of claim
77 wherein said first codeword is $\{+1, -1, +1, +1, -1, +1, +1, +1, -1, -1\}$.

5 81 (Currently amended) The combiner processor of claim
77 wherein said first codeword is $\{-1, +1, -1, -1, +1, -1, -1, +1, +1, +1\}$.

10 82 (Currently amended) The combiner processor of claim
77 wherein said serial stream of baseband symbols includes
Barker codewords.

15 83 (Currently amended) The combiner processor of claim
77 wherein said serial stream of baseband symbols is two
streams of symbols in quadrature phase.

84 (Currently amended) The combiner processor of claim 7
77 wherein said serial stream of quadrature symbols includes
an I channel and a Q channel.

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85 (Currently amended) The combiner processor of claim
77 wherein said training decision function window output has
duration equal to the duration of said codeword.

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Amendment filed under 37 CFR 1.111

Last saved 7/10/2007 11:59:00 AM

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86(Currently amended) The combiner processor of claim
77 wherein said training decision function window output
duration of assertion includes pre-cursor symbols arriving
which arrive prior to the largest said correlation peak in
5 said window output asserted duration.

87(Currently amended) The combiner processor of claim
77 wherein said training decision function window output
duration of assertion includes post-cursor symbols arriving
10 after the largest said correlation peak in said window
output asserted duration.

88(Currently amended) The combiner processor of claim
77 wherein said training decision output indicates which
15 said codeword was received during said window output
asserted duration.

89(Currently amended) The combiner processor of claim
77 wherein said decision input is not asserted during a
20 first interval.

90(Currently amended) The combiner processor of claim
89 wherein said first interval occurs during the preamble of
a received packet.

91 (Currently amended) The combiner processor of claim
89 said first interval is greater than 10 said
codeword symbols.

5 92 (Currently amended) The combiner processor of claim
77 84 wherein said complex conjugate comprises negating the
value of ~~the~~ said Q channel.

10 93 (Currently amended) The combiner processor of claim
77 wherein said channel profile memory is synchronized to
said training decision function window output asserted
duration.

15 94 (Currently amended) The combiner processor of claim
77 wherein said channel profile memory comprises a random
access memory and a memory controller coupled to said random
access memory.

20 95 (Currently amended) The combiner processor of claim
77 wherein said channel profile memory has an in-phase part
and a quadrature part, and said combiner processor adds an
in-phase component of said correlation peak output to said
in-phase channel profile memory and also adds a quadrature
phase component of said correlation peak output to said
25 channel profile memory quadrature part at all times.

Amendment filed under 37 CFR 1.111

96 (Currently amended) The combiner processor of claim
77 wherein said channel profile memory is initialized.

5 97 (Currently amended) The combiner processor of claim
77 wherein said channel profile memory has a number of
locations equal to the number of samples in said codeword.

10 98 (Currently amended) The combiner processor of claim
77 wherein said accumulator includes a memory which is
initialized at the start of each said window output
assertion.

15 99 (Currently amended) The combiner processor of claim
77 wherein said accumulator includes a memory and an adder
which adds the current said multiplier output to said memory
contents.

20 100 (Currently amended) The combiner processor of claim
77 wherein said decision output compares said accumulated
value against a threshold at the end of said window output
assertion.

25 101 (Currently amended) The combiner processor of claim
100 wherein said threshold is 0.

Amendment filed under 37 CFR 1.111

102 (Currently amended) The combiner processor of claim
1 wherein said codewords are used for direct sequence spread
spectrum communications.

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103 (Currently amended) The combiner processor of claim
26 wherein said codewords are used for direct sequence
spread spectrum communications.

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104 (Currently amended) The combiner processor of claim
52 wherein said codewords are used for direct sequence
spread spectrum communications.

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105 (Currently amended) The combiner processor of claim
77 wherein said codewords are used for direct sequence
spread spectrum communications.

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